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10/783,112	02/20/2004	Michael Tayler	200310901-1	7700

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EXAMINER	
MEHRMANESH, ELMIRA	

ART UNIT	PAPER NUMBER
2113	

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Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/783,112	TAYLER ET AL.	
	Examiner	Art Unit	
	Elmira Mehrmanesh	2113	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 February 2004*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-33* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-33* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 February 2004* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

The application of Tayler et al., for a "Timeout event trigger generation" filed February 20, 2004, has been examined.

Claims 1-33 are presented for examination.

Information disclosed and listed on PTO 1449 has been considered.

Claims 1-20, 23, 27-33 are rejected under 35 USC § 102.

Claims 21, 22, 24-26 are rejected under 35 USC § 103.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

Claims 1-20, 23, 27-33 are rejected under 35 U.S.C. 102(b) as being anticipated by Bailey et al. (U.S. Patent No. 5,012,435).

As per claim 1, Bailey discloses a device comprising: an overflow generator to generate a plurality of overflow signals (Fig. 1, elements 61-64) having a plurality of periods (Fig. 5); a plurality of control registers storing a plurality of selection values (Fig. 8, elements 510A-C); and a first trigger generator comprising first trigger generation means for generating a first timeout event trigger signal based on the plurality of

overflow signals and a first one of the plurality of selection values (Fig. 2).

As per claim 2, Bailey discloses plurality of control registers further stores a plurality of control values (Fig. 8, elements 510A-C) and wherein the first trigger generation means comprises means for generating the first timeout event trigger signal (Fig. 2) based on the plurality of overflow signals, the first one of the plurality of selection values, and a first one of the plurality of control values (Fig. 4, element 104).

As per claim 3, Bailey discloses a second trigger generator comprising second trigger generation means for generating a second timeout event trigger signal based on the plurality of overflow signals and a second one of the plurality of selection values (Fig. 3, element 90).

As per claim 4, Bailey discloses the plurality of control registers further stores a plurality of control values (Fig. 8, elements 510A-C), and wherein the second trigger generation means comprises means for generating the second timeout event trigger signal based on the plurality of overflow signals, the second one of the plurality of selection values, and a second one of the plurality of control values (Fig. 2 and 3).

As per claim 5, Bailey discloses the first trigger generation means comprises: means for identifying a first one of the plurality of overflow signals (Fig. 1, elements 61-64) based on the first one of the plurality of selection signals (Fig. 1, elements 22, 24);

means for identifying a period of the first one of the plurality of overflow signals (Fig. 5); and means for generating the first timeout event trigger signal based on the period of the first one of the plurality of overflow signals (Fig. 2).

As per claim 6, Bailey discloses the means for generating the first timeout event trigger signal based on the period of the first one of the plurality of overflow signals comprises means for asserting the first timeout event trigger signal if the period of the first one of the plurality of overflow signals has elapsed since the first trigger generator was last reset (Fig. 3).

As per claim 7, Bailey discloses the plurality of control registers further stores a plurality of control values (Fig. 8, elements 510A-C), and wherein the first trigger generation means comprises: means for identifying a first one of the plurality of overflow signals based on the first one of the plurality of selection signals (Fig. 2); and means for generating the first timeout event trigger signal based on the first one of the plurality of overflow signals and a first one of the plurality of control signals (Fig. 2 and 3).

As per claim 8, Bailey discloses wherein C is the first one of the plurality of control values, and wherein the means for generating the first timeout event trigger signal based on the first one of the plurality of overflow signals and a first one of the plurality of control signals (Fig. 2) comprises: means for asserting the first timeout event trigger signal if the first one of the plurality of overflow signals has been asserted at

least C+1 times since a first predetermined reset event; and means for deasserting the first timeout event trigger signal otherwise (Fig. 3).

As per claim 9, Bailey discloses wherein C is the first one of the plurality of control values, wherein P is the period of the first one of the plurality of overflow signals (Fig. 5), and wherein the means for generating the first timeout event trigger signal based on the first one of the plurality of overflow signals and a first one of the plurality of control signals (Fig. 2) comprises: means for asserting the first timeout event trigger signal if an amount of time at least equal to PC has elapsed since a predetermined reset event; and means for deasserting the first timeout event trigger signal otherwise (Fig. 3).

As per claim 10, Bailey discloses a device comprising: an overflow generator to generate a plurality of overflow signals (Fig. 1, elements 61-64) having a plurality of periods (Fig. 5); a plurality of control registers storing a plurality of selection values and a plurality of control values (Fig. 8, elements 510A-C); a first trigger generator comprising first trigger generation means for generating a first timeout event trigger signal based on the plurality of overflow signals (Fig. 2), a first one of the plurality of selection values (Fig. 1, elements 22, 24), and a first one of the plurality of control values; and a second trigger generator comprising second trigger generation means for generating a second timeout event trigger signal based on the plurality of overflow signals, a second one of the plurality of selection values, and a second one of the

plurality of control values (Fig. 3).

As per claim 11, Bailey discloses a method comprising steps of: (A) generating a plurality of overflow signals (Fig. 1, elements 61-64) having a plurality of periods (Fig. 5);

(B) generating plurality of selection values (Fig. 1, elements 22, 24)

(C) generating a first timeout event trigger signal based on the plurality of overflow signals and a first one of the plurality of selection values (Fig. 2).

As per claim 12, Bailey discloses a step of: (D) generating a plurality of control values; and wherein the step (C) comprises a step of generating the first timeout event trigger signal based on the plurality of overflow signals, the first one of the plurality of selection values, and a first one of the plurality of control values (Fig. 2).

As per claim 13, Bailey discloses a step of: (D) generating a second timeout event trigger signal based on the plurality of overflow signals and a second one of the plurality of selection values (Fig. 3).

As per claim 14, Bailey discloses a step of: (E) generating a plurality of control values (Fig. 1); and wherein the step (D) comprises a step of generating the second timeout event trigger signal based on the plurality of overflow signals, the second one of

the plurality of selection values, and a second one of the plurality of control values (Fig. 3).

As per claim 15, Bailey discloses the step (C) comprises steps of: (C)(1) identifying a first one of the plurality of overflow signals (Fig. 1, elements 61-64) based on the first one of the plurality of selection signals (Fig. 1, elements 22, 24)
(C)(2) identifying a period of the first one of the plurality of overflow signals (Fig. 5)
(C)(3) generating the first timeout event trigger signal based on the period of the first one of the plurality of overflow signals (Fig. 2).

As per claim 16, Bailey discloses the step (C)(3) comprises a step of asserting the first timeout event trigger signal if the period of the first one of the plurality of overflow signals has elapsed since a first predetermined reset event (Fig. 3).

As per claim 17, Bailey discloses a step of: (D) generating a plurality of control values (Fig. 1, elements 22, 24)

and wherein the step (C) comprises steps of: (C)(1) identifying a first one of the plurality of overflow signals (Fig. 1, elements 61-64) based on the first one of the plurality of selection signals (Fig. 1, elements 22, 24)

and (C)(2) generating the first timeout event trigger signal based on the first one of the plurality of overflow signals and a first one of the plurality of control signals (Fig.

2).

As per claim 18, Bailey discloses the first one of the plurality of control signals represents a value C, and wherein the step (C)(2) comprises steps of: (C)(2)(1) asserting the first timeout event trigger signal if the first one of the plurality of overflow signals has been asserted at least (C+1) times since a first predetermined reset event (Fig. 3); and (C)(2)(2) deasserting the first timeout event trigger signal otherwise (Fig. 3).

As per claim 19, Bailey discloses the first one of the plurality of control signals represents a value C, wherein P is the period of the first one of the plurality of overflow signals (Fig. 5), and wherein the step (C)(2) comprises steps of: (C)(2)(1) asserting the first timeout event trigger signal if an amount of time at least equal to PC has elapsed since a predetermined reset event; and (C)(2)(2) deasserting the first timeout event trigger signal otherwise (Fig. 3).

As per claim 20, Bailey discloses a method comprising steps of: (A) generating a plurality of overflow signals (Fig. 1, elements 61-64) having a plurality of periods (Fig. 5);

(B) generating plurality of selection values (Fig. 1, elements 22, 24)

(C) generating a plurality of control values (Fig. 1)

(D) generating a first timeout event trigger signal based on the plurality of overflow signals, a first one of the plurality of selection values, and a first one of the plurality of control values (Fig. 2)

(E) generating a second timeout event trigger signal based on the plurality of overflow signals, a second one of the plurality of selection values, and a second one of the plurality of control values (Fig. 3).

As per claim 23, Bailey discloses a device comprising: selection means comprising means for receiving a plurality of overflow signals (Fig. 1, elements 61-64), means for receiving a selection signal (Fig. 2), means for selecting one of the plurality of overflow signals based on the selection signal (Fig. 2), and means for providing as output the selected one of the plurality of overflow signals (Fig. 1, elements 61-64)

counting means for counting the number of times the selected one of the plurality of overflow signals has been asserted since a predetermined reset event (Fig. 1, element 30)

and timeout event trigger signal generation means for asserting a timeout event trigger signal when the selected one of the plurality of overflow signals has been asserted twice since the predetermined reset event (Fig. 2 and 3).

As per claim 27, Bailey discloses a device comprising: selection means comprising means for receiving a plurality of overflow signals, means for receiving a selection signal, means for selecting one of the plurality of overflow signals based on

the selection signal, and means for providing as output the selected one of the plurality of overflow signals (Fig. 1, elements 61-64)

counting means for counting the number of times the selected one of the plurality of overflow signals has been asserted since a predetermined reset event (Fig. 1, element 30)

comparison means for generating a comparison signal indicating whether a predetermined control value is at least equal to the number of times the selected one of the plurality of overflow signals has been asserted since a predetermined reset event (Fig. 1, element 50)

timeout event trigger signal generation means for asserting a timeout event trigger signal when the predetermined control value is at least equal to the number of times the selected one of the plurality of overflow signals has been asserted since a predetermined reset event (Fig. 2 and 3).

As per claim 28, Bailey discloses a latch comprising means for receiving a clock signal (Fig. 1, element 40), means for receiving the first timeout event trigger signal, and means for providing the timeout event trigger signal as output in response to a transition in the clock signal (Fig. 2 and 3).

As per claim 29, Bailey discloses a method comprising steps of: (A) receiving a plurality of overflow signals (Fig. 1, elements 61-64) having a plurality of periods (Fig. 5);

(B) receiving a first selection signal (Fig. 1, elements 22, 24)

(C) identifying a first one of the plurality of overflow signals based on the first selection signal; and (D) generating a first trigger signal based on the identified one of the plurality of overflow signals (Fig. 2 and 3).

As per claim 30, Bailey discloses the step (D) comprises a step of asserting the first timeout event trigger signal if an amount of time at least equal to the period of the first one of the plurality of overflow signals has elapsed since a first predetermined reset event (Fig. 2 and 3).

As per claim 31 Bailey discloses a step of: (E) receiving a first control signal; and wherein the step (D) comprises a step of generating the first trigger signal based on the first control signal and the identified one of the plurality of overflow signals (Fig. 2).

As per claim 32, Bailey discloses the first one of the plurality of control signals represents a value C, and wherein the step (D) comprises steps of: (D)(1) asserting the first timeout event trigger signal if the first one of the plurality of overflow signals has been asserted at least C+1 times since a first predetermined reset event; and (D)(2) deasserting the first timeout event trigger signal otherwise (Fig. 2 and 3).

As per claim 33, Bailey discloses the first one of the plurality of control signals represents a value C, wherein P is the period (Fig. 5) of the first one-of the plurality of

overflow signals (Fig. 1, elements 61-64), and wherein the step (D) comprises steps of: (D)(1) asserting the first timeout event trigger signal if an amount of time at least equal to PC has elapsed since a predetermined reset event; and (D)(2) deasserting the first timeout event trigger signal otherwise (Fig. 2 and 3).

Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

The factual inquiries set forth in *Graham* **v.** *John Deere Co.*, 383 U.S. 1, 148 USPQ 459 (1966), that are applied for establishing a background for determining obviousness under 35 U.S.C. 103(a) are summarized as follows:

1. Determining the scope and contents of the prior art.
2. Ascertaining the differences between the prior art and the claims at issue.
3. Resolving the level of ordinary skill in the pertinent art.
4. Considering objective evidence present in the application indicating obviousness or nonobviousness.

Claims 21, 22, 24-26 are rejected under 35 U.S.C. 103(a) as being unpatentable over Bailey et al. (U.S. Patent No. 5,012,435) in view of Tamura et al. (U.S. Patent No. 6,247,138).

As per claim 21, Bailey discloses a device comprising: a multiplexer comprising a plurality of data inputs to receive a plurality of overflow signals, a selection input to receive a selection signal and an output to provide one of the plurality of overflow signals selected by the selection signal (Fig. 1)

a one-bit counter comprising a data input coupled to the output of the multiplexer (Fig. 1, element 30), a reset input, and a data output to provide a one-bit count signal;

Bailey fails to explicitly disclose an AND gate.

Tamura teaches:

an AND gate having a first input coupled to the data output of the one-bit counter, a second input coupled to the output of the multiplexer, and an output to provide a first timeout event trigger signal (Fig. 3, element 36).

As per claim 22, Bailey fails to explicitly disclose an AND gate.

Tamura teaches:

a latch comprising a data input coupled to the output of the AND gate, and an output to provide a second timeout event trigger signal (Fig.10).

As per claim 24, Bailey fails to explicitly disclose an AND gate.

Tamura teaches:

a latch comprising means for receiving a clock signal, means for receiving the first timeout event trigger signal, and means for providing the timeout event trigger signal as output in response to a transition in the clock signal (Fig.10).

As per claim 25, Bailey discloses a device comprising: a multiplexer comprising a plurality of data inputs to receive a plurality of overflow signals, a selection input to receive a selection signal, and an output to provide one of the plurality of overflow signals selected by the selection signal (Fig. 1) a multi-bit counter comprising a data input coupled to the output of the multiplexer, a reset input, and a plurality of data outputs to provide a multi-bit count signal (Fig. 1, element 30) a multi-bit comparator having a first plurality of inputs coupled to the plurality of data outputs of the multi-bit counter (Fig. 1, element 50), a second plurality of inputs to receive a multi-bit control signal, and a data output to provide a comparison signal indicating whether the multi-bit count signal is equal to the multi-bit control signal (Fig. 3)

Bailey fails to explicitly disclose an AND gate.

Tamura teaches:

and an AND gate having a first input coupled to the data output of the multi-bit comparator, a second input coupled to the output of the multiplexer, and an output to provide a first timeout event trigger signal (Fig. 3, element 36).

As per claim 26, Bailey fails to explicitly disclose an AND gate.

Tamura teaches:

a latch comprising a data input coupled to the output of the AND gate, and an output to provide a second timeout event trigger signal (Fig.10).

It would have been obvious to one of ordinary skill in the art at the time the invention to use the multiple timer circuit of Bailey et al.'s in combination with the Timing signal generating circuit of Tamura et al. to improve the performance of the circuit.

One of ordinary skill in the art at the time the invention would have been motivated to make the combination because Bailey et al. discloses a multiple event timer circuit. This timer circuit has the capability to monitor a multiple of timeout periods and provide either a general single timeout signal or a specific timeout signal upon the occurrence of each timeout period (Fig. 1). Tamura et al. discloses a timing adjusting circuit which generates n different clocks that are respectively shifted in phase with respect to a supplied reference clock (Fig. 2).

Related Prior Art

The following prior art is considered to be pertinent to applicant's invention, but nor relied upon for claim analysis conducted above.

Liencres (U.S. Patent No. 5,287,362), "Mechanism for implementing multiple time-outs".

Lin et al. (U.S. Patent No. 5,651,113), "Method and apparatus for indicating a time-out by generating a time stamp for an input/output (I/O) channel whenever the channel processes an instruction".

Dien (U.S. Patent No. 6,112,320), "Computer watchdog timer".

Conclusion

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Elmira Mehrmanesh whose telephone number is (571) 272-5531. The examiner can normally be reached on 8-5 M-F.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Robert W. Beausoliel can be reached on (571) 272-3645. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

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